UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,961	01/05/2004	Jiann-Jyh (James) Lay	58268.00327	2032

32294 7590 04/05/2007

SQUIRE, SANDERS & DEMPSEY L.L.P.
14TH FLOOR
8000 TOWERS CRESCENT
TYSONS CORNER, VA 22182

EXAMINER	
WILSON, YOLANDA L	
ART UNIT	**PAPER NUMBER**
2113	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,961	LAY, JIANN-JYH (JAMES)	
	Examiner	Art Unit	
	Yolanda L. Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-16,18 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-16,18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-6,10,11,14-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang (USPN 6728910B1). As per claims 1,10, Huang discloses determining if a memory is functional based on memory BIST data in column 8, lines 50-63; selecting a redundant memory section if a portion of the memory is determined to be nonfunctional in column 8, lines 63-67; determining if at least the selected redundant memory is functional according to a BIST in column 9, lines 6-13; selecting alternate redundant memory sections, if the selected redundant memory section is non-functional, until at least one of the memory is determined to be functional or all redundant memory section have been selected in column 50-67.

Huang discloses updating the redundant memory data structure to indicate that the selected redundant memory section is no longer redundant in column 3, lines 53-58. The redundant memory section is no longer redundant when it is used to replace a faulty row.

3. As per claim 2, Huang discloses further comprising storing data indicating the selected redundant memory section in column 8, lines 65-67.

4. As per claim 3, Huang discloses further comprising outputting a pass or fail signal based on the determining if at least the selected redundant memory is functional according to a BIST in column 9, lines 10-13.

5. As per claim 4, Huang discloses wherein the redundant memory section includes a column or row in column 8, lines 63-67.

6. As per claim 5, Huang discloses wherein the redundant memory section includes a bit in column 5, lines 21-28. All the cells are able to store bits.

7. As per claim 6, Huang discloses wherein the selecting selects a redundant memory section from a redundant memory data structure in column 7, lines 1-2.

8. As per claim 11, Huang discloses a BIST capable of determining if a memory is functional in column 8, lines 50-63; and self-adaptive logic, communicatively coupled to the BIST, capable of selecting a redundant memory section if a portion of the memory is determined to be nonfunctional in column 8, lines 61-67; wherein the BIST is further capable of determining if at least the selected redundant memory is functional in column 9, lines 6-13. The self-adaptive logic is the BISR; selecting alternate redundant memory sections, if the selected redundant memory section is non-functional, until at least one of the memory is determined to be functional or all redundant memory section have been selected in column 8, lines 50-67.

Huang discloses updating the redundant memory data structure to indicate that the selected redundant memory section is no longer redundant in column 3, lines 53-58.

The redundant memory section is no longer redundant when it is used to replace a faulty row.

9. As per claim 14, Huang discloses wherein the redundant memory section includes a column or row in column 8, lines 63-67.

10. As per claim 15, Huang discloses wherein the redundant memory section includes a bit in column 5, lines 21-28. All the cells are able to store bits.

11. As per claim 16, Huang discloses further comprising a redundant memory data structure listing redundant memory sections and wherein the self-adaptive logic selects a redundant memory section from the redundant memory data structure in column 8, lines 61-67.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Huang (US Publication Number 20020136066A1). As per claim 12, Huang '910 discloses further comprising self-adaptive logic and wherein the self-adaptive logic is further capable of storing data indicating the selected redundant memory section in column 8, lines 61-67. The register is the lookup table and the repair table.

Huang '910 fails to explicitly state the self-adaptive logic coupled to a register and storing redundant memory section in the register. Huang '910 discloses a lookup table and repair table that performs the registers functions.

Huang '066 discloses the register on page 6, paragraphs 0047 and 0048.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the self-adaptive logic coupled to a register and storing redundant memory section in the register. A person of ordinary skill in the art would have been motivated to have the self-adaptive logic coupled to a register and storing redundant memory section in the register because register is used to store redundant row information pertaining to whether the row is functioning or not.

14. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Tanizaki et al. (USPN 6993696B1). As per claim 13, Huang '910 discloses further comprising a pin and wherein the self-adaptive logic if further capable of outputting a pass or fail signal based on the BIST determination of the functionality of the selected redundant memory in column 9, lines 10-13.

Huang '910 fails to explicitly state a pin.

Tanizaki et al. discloses a pin in column 10, lines 35-45.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a pin. A person of ordinary skill in the art would have been motivated to have a pin because a pin outputs pass/fail information concerning a memory test.

15. Claims 8,18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang '910 in view of Aipperspach et al. (USPN 6181614B1). As per claims 8,18, Huang '910 fails to explicitly state wherein the method is performed during a manufacturing process.

Aipperspach et al. discloses this limitation in column 5, lines 1-10.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have wherein the method is performed during a manufacturing process. A person of ordinary skill in the art would have been motivated to have wherein the method is performed during a manufacturing process because during the manufacturing process faults and how to repair faults are determined during testing.

16. Claims 9,19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang '910 in view of Cheston et al. (US Publication Number 20030014619A1). As per claims 9,19, Huang '910 fails to explicitly state wherein the method is performed during power up of an integrated circuit.

Cheston et al. discloses this limitation on page 3, paragraph 0026.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have wherein the method is performed during power up of an integrated circuit. A person of ordinary skill in the art would have been motivated to have wherein the method is performed during power up of an integrated circuit because during power up the validity of the memory is determined.

Response to Arguments

17. Applicant's arguments filed 02/20/2007 have been fully considered. Applicant argues on pages 9-10, under the Remarks section, "However, nowhere in the testing process described in Huang '910 is there any teaching or discussion of selecting alternate redundant memory sections, if the selected redundant memory section is non-functional, until at least one of the memory is determined to be functional or all redundant memory section have been selected and updating the redundant memory data structure...Further supporting Applicant's position...a second test is performed to check the redundant memory."

Examiner respectfully disagrees. The 'selected redundant memory' is the memory that is subject to testing by the testing scheme disclosed in Huang '910. The good rows have already been tested and the faulty rows are failed over to good redundant rows. The 'updating the redundant memory data structure' is the repair table which keeps track of whether or not the redundant memory location is being used for each of the memory locations as disclosed in Huang '910. This can be seen in column 8, lines 50-67. The rows are rechecked in order to make sure that the redundant rows as well as the previously determined good rows are functioning properly.

Applicant argues on page 12, under the Remarks section, "A BISR 'Wrapper' system interfaces the BIST engine to the BISR repair circuitry...With the Wrapper, BISR operation need no longer be closely coupled to the operation or internal structure of the BIST. Consequently, modification of the BIST mechanism, e.g., to improve fault coverage, can be implemented without influencing the BISR. However, Huang '066

does not teach, show, or suggest a BIST that is capable of selecting... updating the redundant memory data structure to indicate that the selected redundant memory section is no longer redundant, as recited in claim 11, the independent claim from which claim 12 depends ..."

Examiner respectfully disagrees. Huang '066 reference was used to reject the register limitation. As indicated in Huang '066, the register is associated with the BISR, which is used with the BIST; therefore, the BISR would be influenced by the register being modified. Please see the arguments presented above concerning the updating the data structure.

Applicant argues on page 14, under the Remarks section, "However,... Tanizaki does not teach, or suggest a BIST that is capable of updating the redundant memory data structure to indicate that the selected redundant memory section is no longer redundant, as recited in claim 11, the independent claim from which claim 13 depends..."

Examiner respectfully disagrees. Please see the arguments presented above concerning the selecting alternate redundant memory sections and updating the data structure.

Applicant argues on page 15, under the Remarks section, "However,... Aipperspach does not teach or suggest a BIST that is capable of updating the redundant memory data structure to indicate that the selected redundant memory section is no longer redundant, as recited in claims 1 and11, the independent claim from which claims 8 and 18 depend..."

Examiner respectfully disagrees. Please see the arguments presented above concerning the updating the data structure.

Applicant argues on page 17, under the Remarks section, "However,... Cheston does not teach, show, or suggest a BIST that is capable of updating the redundant memory data structure to indicate that the selected redundant memory section is no longer redundant, as recited in claims 1 and11, the independent claim from which claims 9 and 19 depend. As such, Applicant submits that Aipperspach does not further the teaching of the Huang references to the level necessary to properly support an obviousness rejection..."

Examiner respectfully disagrees. Please see the arguments presented above concerning the selecting the redundant memory sections and updating the data structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda L. Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Yolanda L Wilson
Examiner
Art Unit 2113